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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,124	08/25/2003	Aurelian Vasile Lazarut	X-1391 US	3211

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EXAMINER	
LEVIN, NAUM B	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,124	LAZARUT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-13 and 15-30* is/are pending in the application.

4a) Of the above claim(s) *11-13,15 and 26-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/648,124, Amendment filed on 07/21/2006 and Response to election/restriction filed on 10/31/2006. Applicants have amended claims 1, 6, 16 and 21, and include additional limitations, such as: "each system under test of said plurality of systems under test has a different programmable logic device architecture"; a selected system under test". Claims 9 and 14 have been canceled.

2. By amending independent claims 1, 6, 16 and 21, which necessitates a changing the ground for rejection, and the fact that claims 2-5, 7-8, 10, 17-20 and 22-25 are dependent from claims 1, 6, 16 and 21 accordantly, the new rejection of claims 1-8, 10 and 16-25 was necessitated by applicant's amendment.

3. Applicant has provisionally elected claims 1-8, 10 and 16-25 (Group 1) with traverse. Claims 11-13, 15 and 26-30 (Group 2) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/31/2006.

4. The possible inventions of Group 1 (claims 1-8, 10 and 16-25) and Group 2 (claims 11-13, 15 and 26-30) related to a client-server semiconductor verification system, but Group 2 includes additional utilities, such as: "**a job distribution server** coupled to said plurality of client computers"; "a server coupled to said plurality of client computers **by way of said job distribution server**"; "**server receiving test job from job distribution server**".

Applicant's Specification also distinguishes these groups as: "Referring specifically to Fig. 1, a block diagram of a system for verifying a semiconductor design according to an embodiment of the present invention is shown. In particular, a plurality of client devices 102 are coupled to a server 104 by way of a network 106 – paragraph 20. ... Another embodiment relates to a system having multiple test servers connected via LAN/WAN to one master server or a computer that will act as a job distribution system for all the SUTs connected to the various test servers – paragraph 32".

Applicant's Specification also recites: "Fig. 1 is a block diagram of a system for verifying a semiconductor design according to an embodiment of the present invention; Fig. 2 is a block diagram of a system for verifying a semiconductor design according to an alternate embodiment of the present invention - paragraphs 8-9".

As such, the restriction is hereby made final.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8, 10 and 16-25 are rejected under 35 U.S.C. 103(a) as being unpatentable by Levi et al. (US Patent 6,363,517) in view of Miller et al. (US Pub. No.: 20020121913).

6. As to claims 1, 6, 16 and 21 Levi discloses:

(1) A client-server semiconductor verification system, said system comprising:

a client computer storing a test job for testing a design of a programmable logic circuit (an apparatus comprises creating respective configuration bitstreams on a data processing system at a first location /the computer at the local site–col.2, ll.41-45), said test job (configuration bitstream 150, Fig. 2) having test vectors and configuration data for said programmable logic circuit (Configuration bitstream 150 includes a group of bit sequences 152 for evolving circuitry, a group of bit sequences 154 for test circuitry – col.6, ll.10-12; the test circuitry could be configured to generate a fixed set of test vectors - col.6, ll.20-21) (col.2, ll.41-45; col.6, ll.10-24);

a server coupled to said client computer by way of a network, said server receiving said test job from said client computer (The configuration bitstreams are downloaded from the data processing system/client to a device or devices at another location, for example via a network –col.2, ll.45-48; At the remote site, a board in a computer holds an FPGA or other programmable device. This remote computer may be on the other side of the world. The two computers may communicate through a local area network, through a modem, or through the internet. A server must be provided at the remote site - col.2, ll.55-61) (col.2, ll.45-50; col.2, ll.55-65); and

a plurality of systems under test coupled to said server (Test circuits are inserted into bitstream 204 to drive test data into the evolved circuit/s (device/s 206 in Fig.3 or devices 404 in Fig.5) – col.6, ll.33-34; Using the device and board identifiers and parameters, the populations can evolve on separate devices. If one device is remote

from another, the transfer can be made over the internet. To accomplish remote internet access requires software on a server or computer to which the remote FPGA is connected – col.11, ll.36-41; The configuration bitstreams are downloaded from the data processing system to a device or devices at another location – col.2, ll.45-47), wherein each system under test has a different programmable logic device architecture (FPGA1 and FPGA2 are both used to evolve a design for a first objective, for example a counter. FPGA3 is used to evolve a controller, for example ... FPGA1 and FPGA2 will be evaluated against whether a particular set of input signals produces output signals expected from a counter, while FPGA3 will be evaluated on whether its output signals match those of the desired controller – col.13, ll.20-29), a programmable logic circuit which is configured with a circuit design implemented according to said configuration data (At the remote site, a board in a computer holds an FPGA or other programmable device –col.2,ll.55-56), said system under test receiving said test vectors and outputting result vectors to the client computer by way of said server (devices at the second location then operate using bitstreams evolved at the first location, and generate results that are sent back to the first location – col.2,ll.48-50; A server must be provided at the remote site to read the incoming bitstream and configure the programmable device. The server also reads state data from the device during or after operation and feeds this data back to the computer at the local site/client – col.2, ll.60-65) (col.2, ll.45-65; col.6, ll.25-50; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60);

(6) A client-server semiconductor verification system, said system comprising:

a client computer storing a test job for testing a design of a programmable logic circuit (an apparatus comprises creating respective configuration bitstreams on a data processing system at a first location /the computer at the local site–col.2, ll.41-45), said test job (configuration bitstream 150, Fig. 2) having test vectors and configuration data for said programmable logic circuit (Configuration bitstream 150 includes a group of bit sequences 152 for evolving circuitry, a group of bit sequences 154 for test circuitry – col.6, ll.10-12; the test circuitry could be configured to generate a fixed set of test vectors - col.6, ll.20-21) (col.2, ll.41-45; col.6, ll.10-24);

a server coupled to said client computer by way of a network, said server receiving said test job from said client computer (The configuration bitstreams are downloaded from the data processing system/client to a device or devices at another location, for example via a network –col.2, ll.45-48; At the remote site, a board in a computer holds an FPGA or other programmable device. This remote computer may be on the other side of the world. The two computers may communicate through a local area network, through a modem, or through the internet. A server must be provided at the remote site - col.2, ll.55-61) (col.2, ll.45-50; col.2, ll.55-65); and

a plurality of systems under test coupled to said server (Test circuits are inserted into bitstream 204 to drive test data into the evolved circuit/s (device/s 206 in Fig.3 or devices 404 in Fig.5) – col.6, ll.33-34; Using the device and board identifiers and parameters, the populations can evolve on separate devices. If one device is remote from another, the transfer can be made over the internet. To accomplish remote internet access requires software on a server or computer to which the remote FPGA is

connected – col.11, ll.36-41; The configuration bitstreams are downloaded from the data processing system to a device or devices at another location – col.2, ll.45-47), wherein each system under test has a different programmable logic device architecture (FPGA1 and FPGA2 are both used to evolve a design for a first objective, for example a counter. FPGA3 is used to evolve a controller, for example ... FPGA1 and FPGA2 will be evaluated against whether a particular set of input signals produces output signals expected from a counter, while FPGA3 will be evaluated on whether its output signals match those of the desired controller – col.13, ll.20-29), a programmable logic circuit which is configured with a circuit design implemented according to said configuration data (At the remote site, a board in a computer holds an FPGA or other programmable device –col.2,ll.55-56), said system under test receiving said test vectors and outputting result vectors to the client computer by way of said server (devices at the second location then operate using bitstreams evolved at the first location, and generate results that are sent back to the first location – col.2,ll.48-50; A server must be provided at the remote site to read the incoming bitstream and configure the programmable device. The server also reads state data from the device during or after operation and feeds this data back to the computer at the local site/client – col.2, ll.60-65) (col.2, ll.45-65; col.6, ll.25-50; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60);

(16) A method of verifying semiconductor design by way of a server, said method comprising:

storing a test job for testing a design of a circuit in a client computer, said test job having test vectors and configuration data for a circuit implemented in programmable logic (col.2, ll.41-45; col.6, ll.10-24);

providing a plurality of systems under test coupled to said server (Test circuits are inserted into bitstream 204 to drive test data into the evolved circuit/s (device/s 206 in Fig.3 or devices 404 in Fig.5) – col.6, ll.33-34; Using the device and board identifiers and parameters, the populations can evolve on separate devices. If one device is remote from another, the transfer can be made over the internet. To accomplish remote internet access requires software on a server or computer to which the remote FPGA is connected – col.11, ll.36-41; The configuration bitstreams are downloaded from the data processing system to a device or devices at another location – col.2, ll.45-47), wherein each system under test has a different programmable logic device architecture (FPGA1 and FPGA2 are both used to evolve a design for a first objective, for example a counter. FPGA3 is used to evolve a controller, for example ... FPGA1 and FPGA2 will be evaluated against whether a particular set of input signals produces output signals expected from a counter, while FPGA3 will be evaluated on whether its output signals match those of the desired controller – col.13, ll.20-29) (col.2, ll.45-65; col.6, ll.25-41; col.6, ll.42-50; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60);

a system under test programmable logic circuit which is configured with a circuit design implemented according to said configuration data (At the remote site, a board in a computer holds an FPGA or other programmable device –col.2,ll.55-56), said system under test receiving said test vectors and outputting result vectors to the client

computer by way of said server (devices at the second location then operate using bitstreams evolved at the first location, and generate results that are sent back to the first location – col.2,ll.48-50; A server must be provided at the remote site to read the incoming bitstream and configure the programmable device. The server also reads state data from the device during or after operation and feeds this data back to the computer at the local site/client – col.2, ll.60-65) (col.2, ll.45-65; col.6, ll.25-50; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60); and

comparing said result vectors from said system under test to expected result vectors (State data 208 is evaluated in accordance with criteria selected to provide an indication of the suitability of configuration bitstream 204 to meet predetermined requirements. For example, state data 208 can be compared to expected results data) (col.2, ll.50-54; col.6, ll.51-60);

(21) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a client computer lo a test sever, said client computer storing a test job for testing the design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit (col.2, ll.41-50; col.2, ll.55-65; col.6, ll.10-24; col.11, ll.34-50);

providing a plurality of systems under test coupled to said server (Test circuits are inserted into bitstream 204 to drive test data into the evolved circuit/s (device/s 206 in Fig.3 or devices 404 in Fig.5) – col.6, ll.33-34; Using the device and board identifiers and parameters, the populations can evolve on separate devices. If one device is

remote from another, the transfer can be made over the internet. To accomplish remote internet access requires software on a server or computer to which the remote FPGA is connected – col.11, ll.36-41; The configuration bitstreams are downloaded from the data processing system to a device or devices at another location – col.2, ll.45-47), wherein each system under test has a different programmable logic device architecture (FPGA1 and FPGA2 are both used to evolve a design for a first objective, for example a counter. FPGA3 is used to evolve a controller, for example ... FPGA1 and FPGA2 will be evaluated against whether a particular set of input signals produces output signals expected from a counter, while FPGA3 will be evaluated on whether its output signals match those of the desired controller – col.13, ll.20-29) (col.2, ll.45-65; col.6, ll.25-50; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60);

reconfiguring a programmable logic circuit according to said configuration data (At the remote site, a board in a computer holds an FPGA or other programmable device –col.2,ll.55-56), said system under test receiving said test vectors and outputting result vectors to the client computer by way of said server (devices at the second location then operate using bitstreams evolved at the first location, and generate results that are sent back to the first location – col.2,ll.48-50; A server must be provided at the remote site to read the incoming bitstream and configure the programmable device. The server also reads state data from the device during or after operation and feeds this data back to the computer at the local site/client – col.2, ll.60-65) (col.2, ll.45-65; col.6, ll.41-67; col.7, ll.1-8; col.9, ll.62-67; col.10, ll.1-2; col.11, ll.35-41; col.13, ll.15-60); and

comparing said result vectors from said system under test to expected result

vectors (col.2, ll.50-54; col.6, ll.51-60).

With respect to claims 1, 6, 16 and 21 Levi teaches the features above but lacks a client-server semiconductor verification system further comprising plurality of client computers, and selecting system under test.

7. As to claims 1, 6, 16 and 21 Miller recites:

A client-server semiconductor verification system further comprising (Abstract):

plurality of client computers (a site host (not shown in FIG. 1) is coupled to multiple cell hosts in order to collect test data from the individual cell hosts. The site host compresses the test data, e.g., into a zip file, and places the data onto a central server – [0034]; Cell host 102 runs the test sequence for each device being tested in trays 101. Thus, cell host 102 controls the testing in all 18 trays. In an exemplary embodiment, as illustrated in FIG. 2, cell host 102 communicates via a network link 201 such as an Ethernet link with each tray. The cell host also provides a graphical user interface for control of tests and trays via display 104 – [0033], Figs.1-2); ([0033]-[0035]); and

selecting a system under test (port de-multiplexer circuit 406 is used to select in hardware which of the tray test boards receives a particular communication - [0037]; The CPU status window in status window 903 provides detailed status information for the selected device under test – [0062], Fig.9) ([0037]; [0062]).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Miller's teaching regarding the client-server semiconductor verification system further comprising plurality of client computers and

selecting system under test, and use it in Levi's invention to provide a tester that allows the testing parameters to be varied for each system under test without affecting the other system under test, thereby increasing an efficiency of the client-server semiconductor verification system.

8. As to claims 2-5, 7-8, 10, 17-20 and 22-25 Levi describes:

(2), (4), (18) The system/method, wherein said client device further has expected results (col.2, ll.50-54);

(3), (17) The system/method, wherein said client device generates said test vectors (col.6, ll.10-24);

(5) The system, wherein said test vectors and said expected results are generated by an external device (col.6, ll.16-24; col.10, ll.25-39);

(7), (23) The system/method, wherein said server comprises a network interface (col.2, ll.55-65);

(8), (10), (19), (20), (24) The system/method, wherein said server comprises a system under test interface (col.2, ll.45-50; col.2, ll.55-65; col.11, ll.35-51);

(22) The method further comprising a plurality of servers coupled to said plurality of client devices (col.11, ll.35-51);

(25) The method of claim 21 wherein said step of comparing comprises comparing said result vectors from said system under test to expected result vectors at said client device (col.2, ll.50-54).

REMARKS

9. The examiner introduces a new ground of rejection that is necessitated by applicant's amendment of the claims, see ***Form Paragraph 7.42.031*** (¶ 7.42.031 Action Is Final, Action Following Submission Under 37 CFR 1.129(a) Filed On Or After June 8, 2005).

10. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

1/20/07

THUAN V. DO
PRIMARY PATENT EXAMINER